Motorcomm YT8821 Product Brief

The YT8821 is a 10BASE-Te, 100BASE-TX, 1000BASE-T and 2.5GBASE-T transceiver highly

integrated into a single monolithic CMOS chip, and is compatible with both the IEEE 802.3

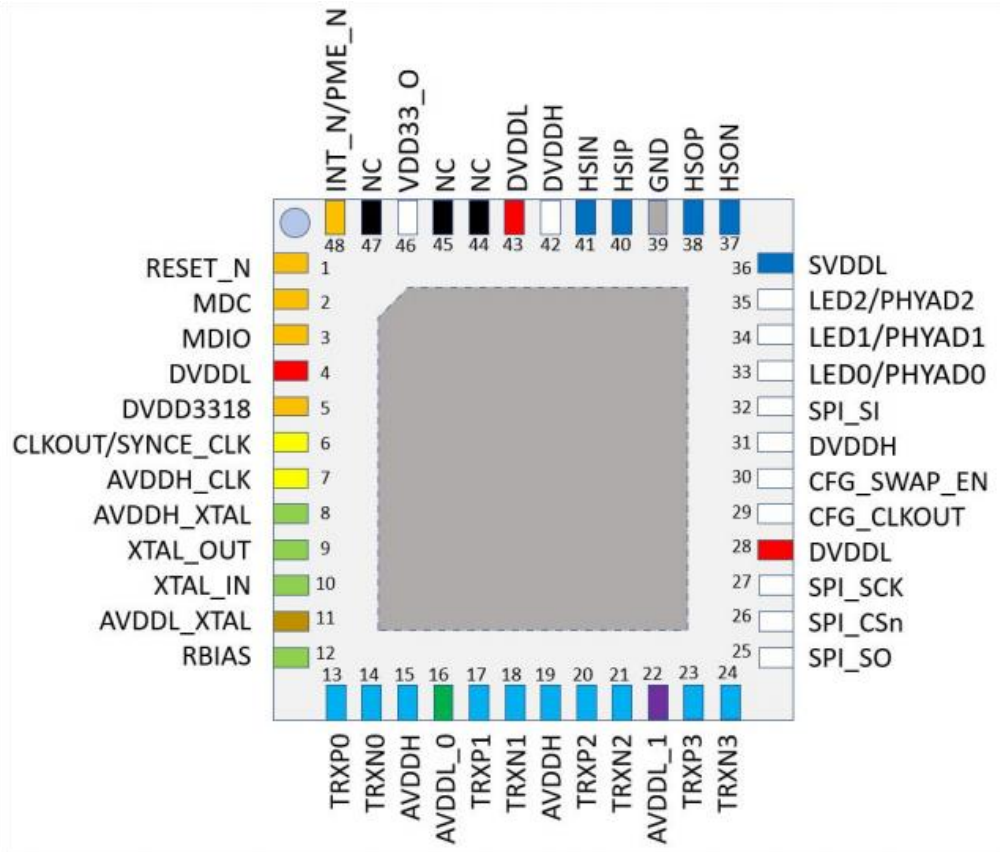standard and

the NBASE-T Alliance PHY .

Overview

YT8821 performs all the necessary physical layer functions for 10BASE-Te, 100BASE-TX,

1000BASE-T and 2.5GBASE-T ethernet over CAT.5e UTP cable.

The YT8821 uses advanced DSP technology and an Analog Front End to enable high-speed data

transmission and reception over UTP cable. It is a highly integrated solution combining digital

adaptive

equalizers, ADCs, line driver, echo cancellers, crosstalk cancellers, phase-locked loops and so on.

Functions such as Crossover Detection & Auto-Correction, polarity correction are also supported.

Data transfer between MAC and YT8821 is by the SERDES interface which can be configured as

SGMII and 2500BASE-X.

YT8821 operates at multiple digital I/O voltages, including 3.3V and 1.8V.

Pin Assignment

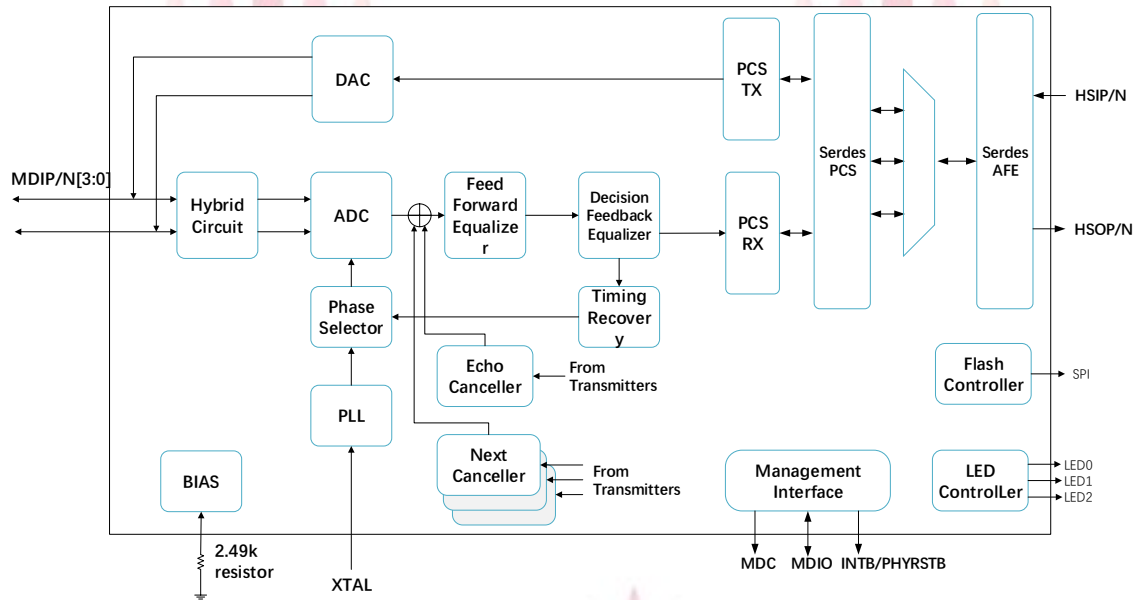| Pin	Signal
48	INT_N/PME_N
47	NC
46	VDD33_O
45	NC
44	NC
43	DVDDL
42	DVDDH
41	HSIN
40	HSIP
39	GND
38	HSOP
37	HSON

Left side:
- 1 RESET_N
- 2 MDC
- 3 MDIO
- 4 DVDDL
- 5 DVDD3318
- 6 CLKOUT/SYNCE_CLK
- 7 AVDDH_CLK
- 8 AVDDH_XTAL
- 9 XTAL_OUT
- 10 XTAL_IN
- 11 AVDDL_XTAL
- 12 RBIAS

Right side:
- 36 SVDDL
- 35 LED2/PHYAD2
- 34 LED1/PHYAD1
- 33 LED0/PHYAD0
- 32 SPI_SI
- 31 DVDDH
- 30 CFG_SWAP_EN
- 29 CFG_CLKOUT
- 28 DVDDL
- 27 SPI_SCK
- 26 SPI_CSn
- 25 SPI_SO

Bottom:
- 13 TRXP0
- 14 TRXN0
- 15 AVDDH
- 16 AVDDL_0
- 17 TRXP1
- 18 TRXN1
- 19 AVDDH
- 20 TRXP2
- 21 TRXN2
- 22 AVDDL_1
- 23 TRXP3
- 24 TRXN3

Block Diagram

Application Diagram

- AUTO_BX2500_SGMII

- FORCE_BX2500

- UTP_TO_FIBER_FORCE

Key Features

- Compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- Supports IEEE 802.3az (Energy Efficient Ethernet)

- Supports IEEE 802.3bz(2.5GBASE-T)

- Supports Full Duplex flow control (IEEE 802.3x)

- Supports IEEE 802.3 optional ability(Fast Retrain)

- Integrated 10BASE-Te, 100BASE-TX, 1000BASE-T and 2.5GBASE-T IEEE 802.3

  Compliant transceiver

- Auto-Negotiation with extended next page capability(XNP)

- Compatible with NBASE-T Alliance PHY Specification

- Supports pair swap/polarity/skew correction

- Crossover detection and auto-correction

- Configurable MDI port ordering(MDI swap) for easy PCB layout

- Supports power down/link down power saving mode

- Supports clause 22 and clause 45 MDC/MDIO management interface

- Supports rate adaptor for SERDES

- Selectable SERDES interface to MAC control(SGMII /2500BASE-X)

- Built-in Wake-on-LAN(WOL) over UTP

- Supports Interrupt function over UTP

- Supports parallel detection

- Baseline Wander Correction

- Supports 3.3/1.8V signaling for MDIO access

- Supports 25MHz crystal or external OSC

- Provides 25MHz clock source for MAC

- Provides 3 network customized LEDs with controllable LED Blinking Frequency and Duty Cycle

- Self-Loopback diagnostic capability

- Supports SPI Flash

Target Applications

- Ethernet Switch

- DTV (Digital TV)

- Communication and Network Riser

- Routers, PON Equipment

- Printer and Office Machine

- MAU(Media Access Unit)