Motorcomm YT8011A/AR/AN Series Product Brief

AUTOMOTIVE 100/1000BASE–T1 ETHERNET TRANSCEIVER

Overview

The YT8011A/AN/AR is a single-pair Ethernet physical layer transceiver that supports operation over unshielded twisted pair (UTP). The transceiver complies with the Ethernet physical layer portion of100/1000BASE-T1 as defined by IEEE 802.3bw and the IEEE 802.3bp standard, including auto-negotiation, link-synchronization and OAM features.

The device supports reduced gigabit media independent interface (RGMII) and serial gigabit media independent interface (SGMII). The YT8011A/AN/AR supports 3.3V/2.5V/1.8V I/O signaling of RGMII. YT8011A/AN supports the signal of SGMII.

The device supports SLEEP/WAKE function for the automotive Ethernet. The SLEEP function implements the PHY into the sleep mode which has lower power consumption. The WAKE function can trigger the PHY and make it efficiently wake up to the normal operation mode from the sleep mode.

The YT8011A/AN/AR uses state-of-the-art mixed-signal technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as adaptive equalization, echo cancellation, data recovery, and error correction are implemented in the YT8011A/AN/AR to provide robust transmission and reception capabilities at 100Mbps, or 1000Mbps. It offers high Electro-Static Discharge (ESD) protection as well as excellent Electromagnetic Compatibility (EMC) performance.

P/N	MAC Interface	AUX Power Input @Sleep Mode	Package
YT8011A	RGMII & SGMII	12V	QFN48 7*7
YT8011AN	RGMII & SGMII	3.3V	QFN48 7*7
YT8011AR	RGMII	3.3V	QFN40 6*6

Application Diagram

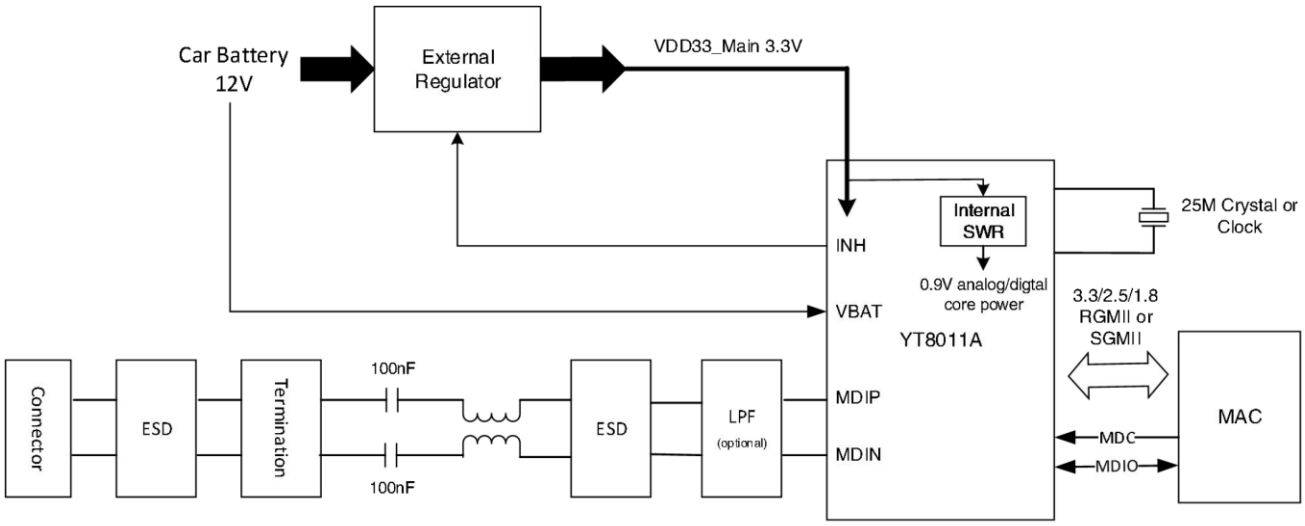

Figure 1. YT8011A Application diagram

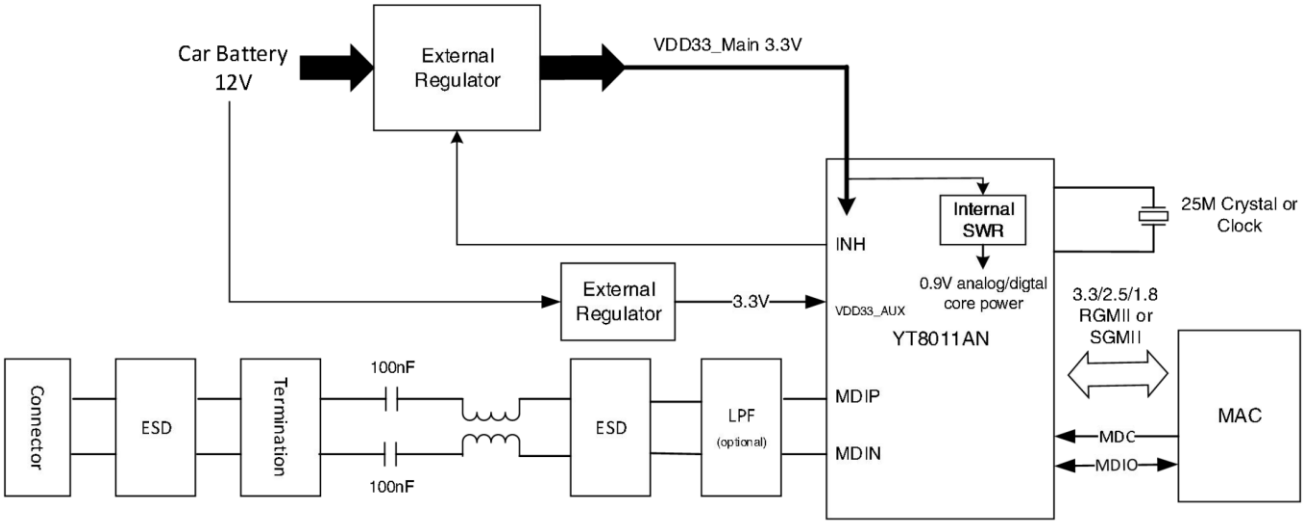

Figure 2.YT8011AN Application diagram

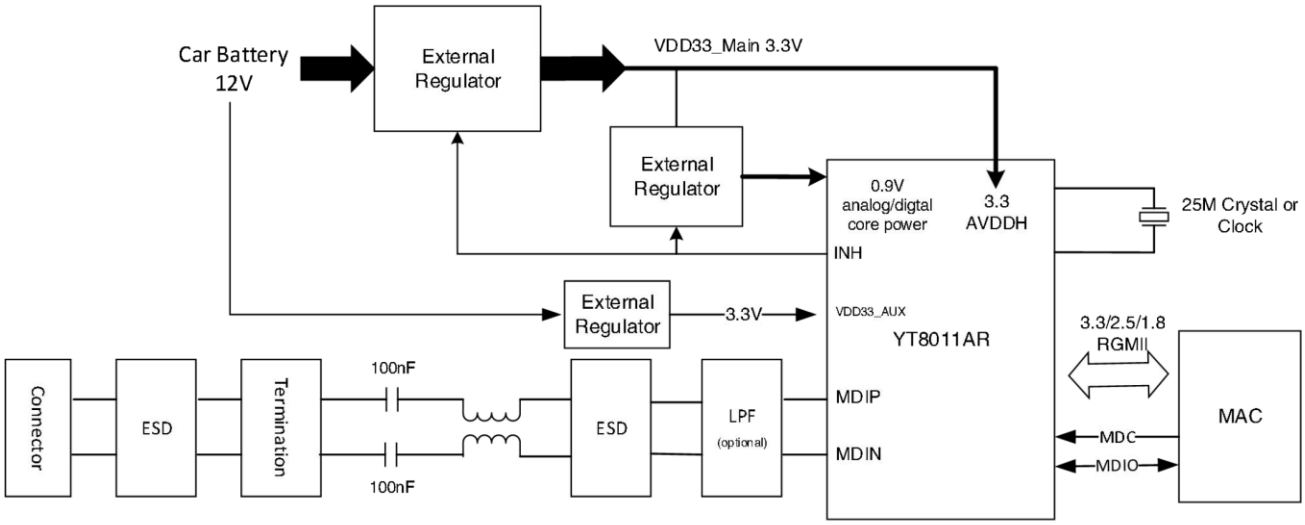

Figure 3.YT8011AR Application diagram

Key Features

- 100/1000BASE-T1
  - Compliant with 100/1000BASE-T1 defined by IEEE 802.3bw and 802.3bp standards
  - Fast link-up time(<100ms)
  - Full duplex supported
  - Auto-negotiation
  - Link Synchronization
- Interface
  - Supports RGMII with optional internal delay on TX and RX path and 1.8V/2.5V/3.3V RGMII IO voltage
  - Supports SGMII (Only for YT8011A/AN)
  - MDC/MDIO management interface
  - Interrupt notifications
  - PTP GPIO
- Precision Time Protocol (PTP)
  - Supports for Precision time protocol, including IEEE1588v1, v2 and 802.1AS
  - PTP packet parser supports layer 2 Ethernet, IPv4/UDP, IPv6/UDP packets
  - One-Step operation supported
  - Adjustable PTP clock for synchronization
  - Deterministic and low transmission latency for PTP mechanism
  - Programmable time application interface through the PTP GPIO
  - Selectable PTP clock input from the external reference clock source
- Clocking
  - Supports 25MHz crystal/external clock
- Power Saving
  - Supports sleep & wake up function
  - Low power consumption at sleep mode < 30uA
  - Supports remote/local wake-up
  - 12V AUX Power Support (Only for YT8011A)
- Performance
  - AEC-Q100 Grade 1(-40℃~125℃)
  - Low Electro-Magnetic Emission
  - Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
  - Advanced digital baseline wander correction
- Packages
  - YT8011A/AN:48pin QFN package (7*7)
  - YT8011AR:40pin QFN package (6*6)

Pin Assignment

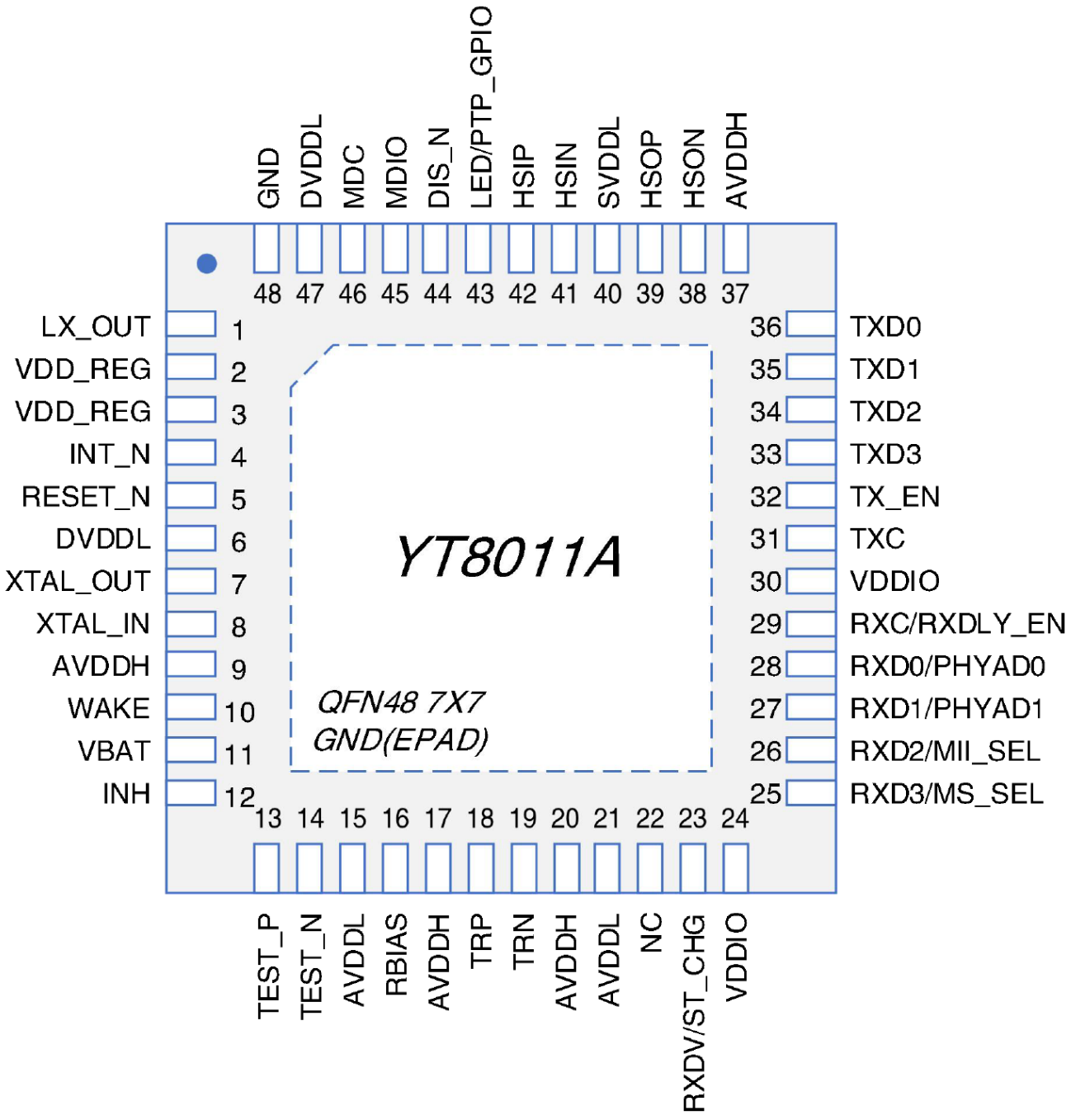

Figure 4. YT8011A Pin Assignment

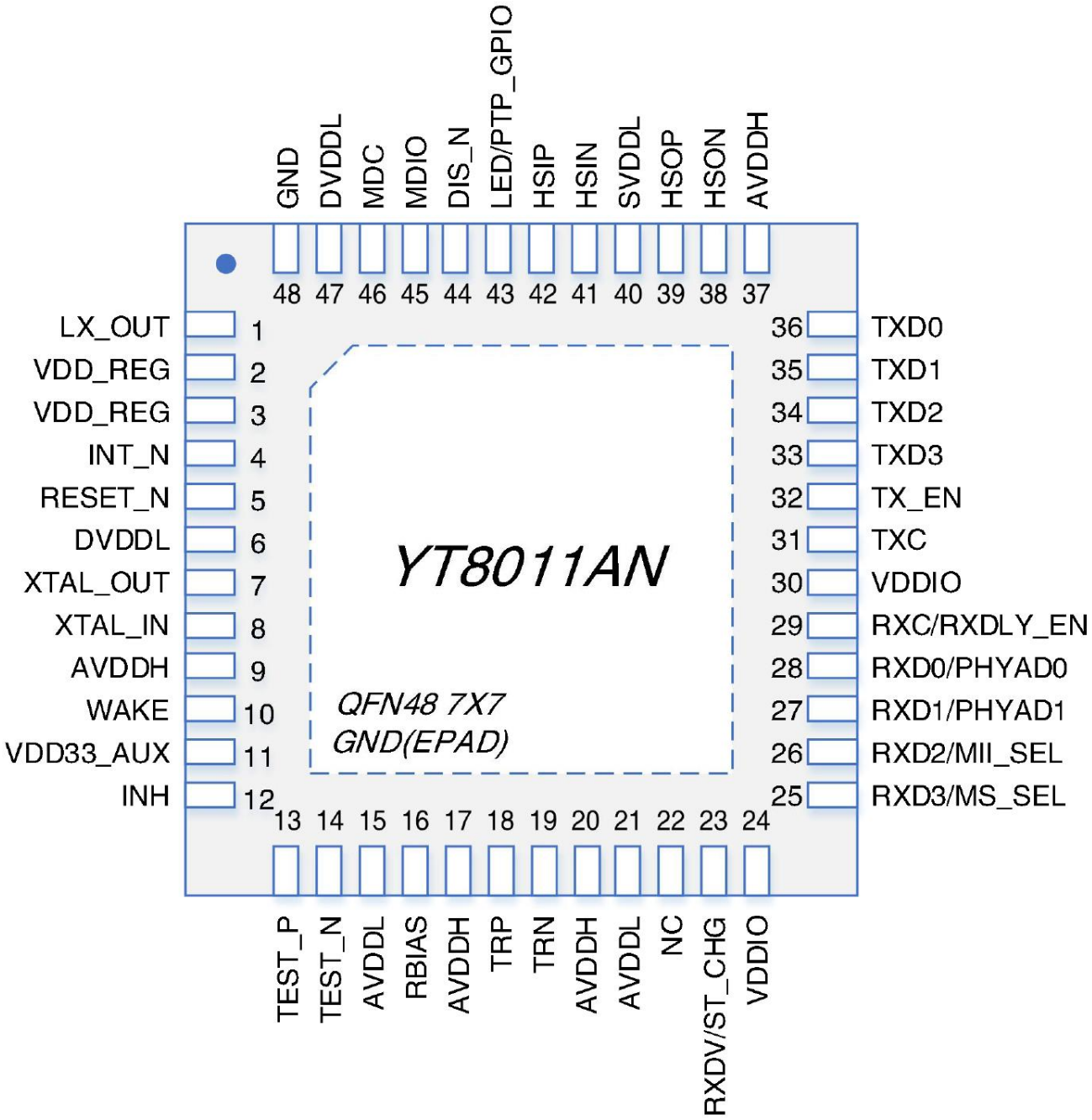

Figure 5. YT8011AN Pin Assignment

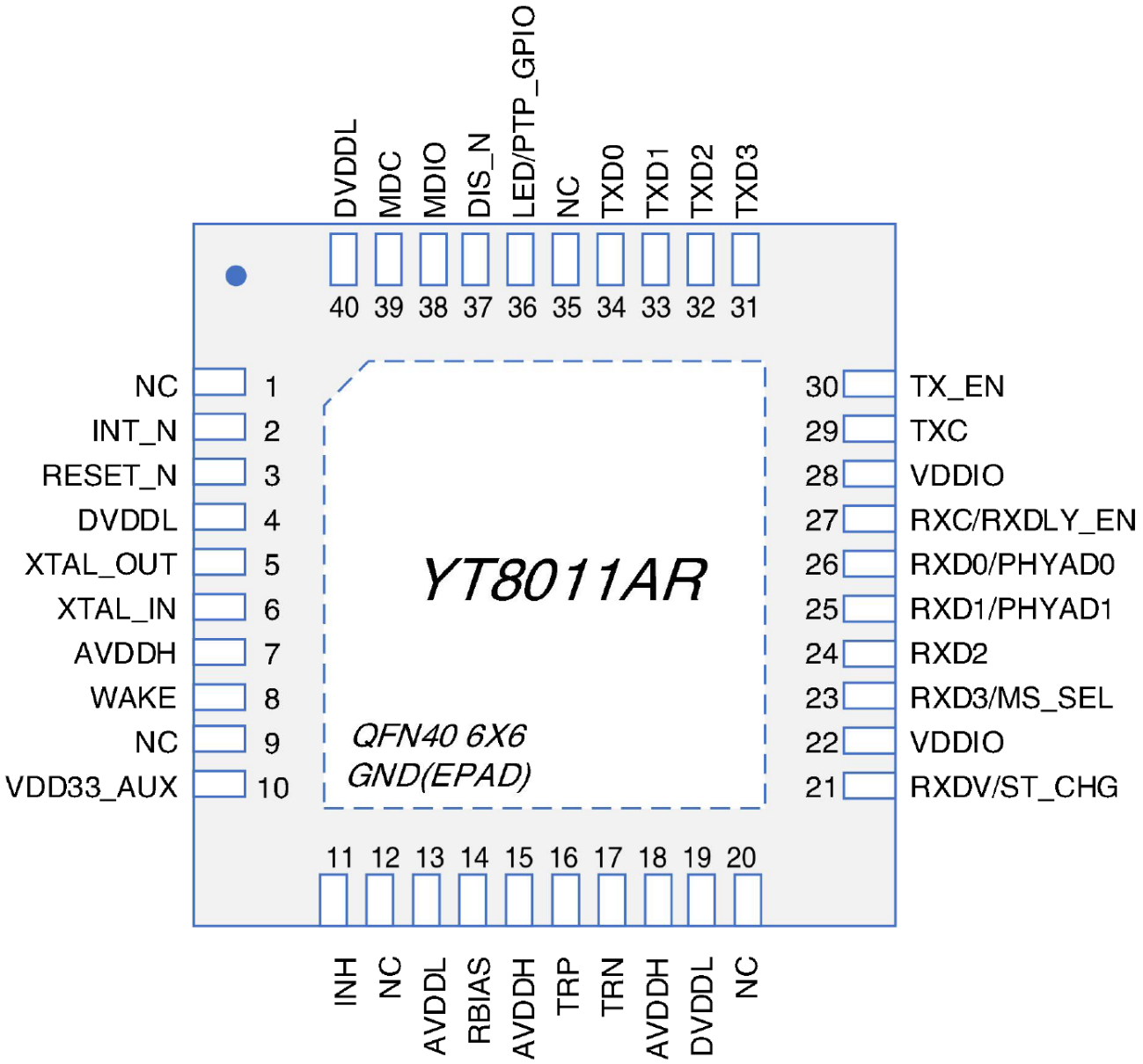

Figure 6. YT8011AR Pin Assignment

Target Applications

- Automotive Infotainment Systems
- Automotive Diagnostics
- Advanced Driver Assistance Systems
- Vehicle Body Control Electronics
- Domain Control Units
- Automotive Switches